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G11B 20/10

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INT CL[6] G11B 20/10
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(54) Memory control in a DVD player

(57) A digital video disk reproducing device utilizes a single memory 320 both for the error correction and for the data buffering. The device designates a unit number to each sector of the memory 320 and determines first, second and third regions. The first region corresponds to an absolute value of a unit number obtained by subtracting a unit number Y of a sector where a data read/write operation is completed during the scrambling from a unit number X of a start sector in an error correction block where the error correction is completed. The second region corresponds to an absolute value of a unit number obtained by subtracting a unit number Z of a sector where the data is completely transferred to the audio/video decoders or the ROM decoder from the unit number Y. The third region corresponds to an absolute value of a unit number obtained by subtracting the unit number Z from a unit number W of a sector where a writing operation of demodulated data is completed. Thereafter, the devices controls a W-pointer and a Z-pointer not to overfull a Z-pointer and a Ypointer respectively, and controls an X-pointer and the Ypointer not to pass ahead the W-pointer and the X-pointer respectively.

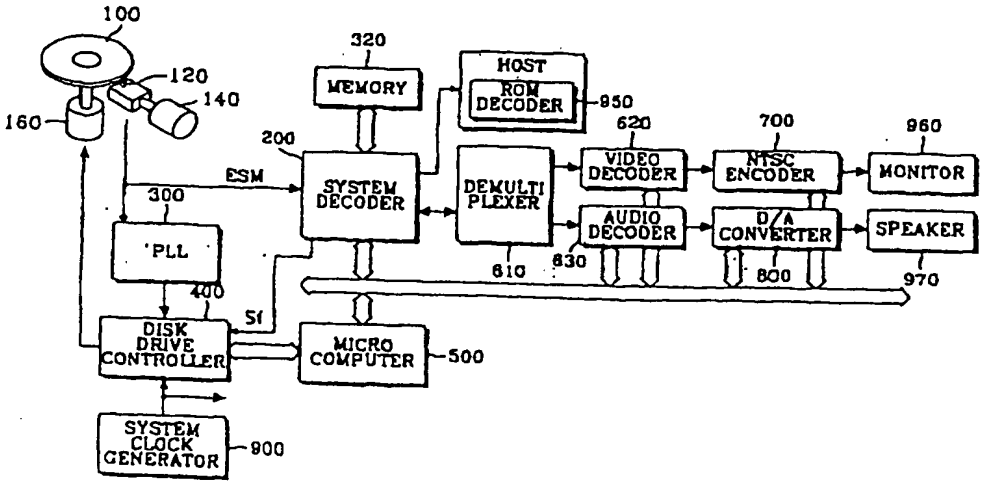
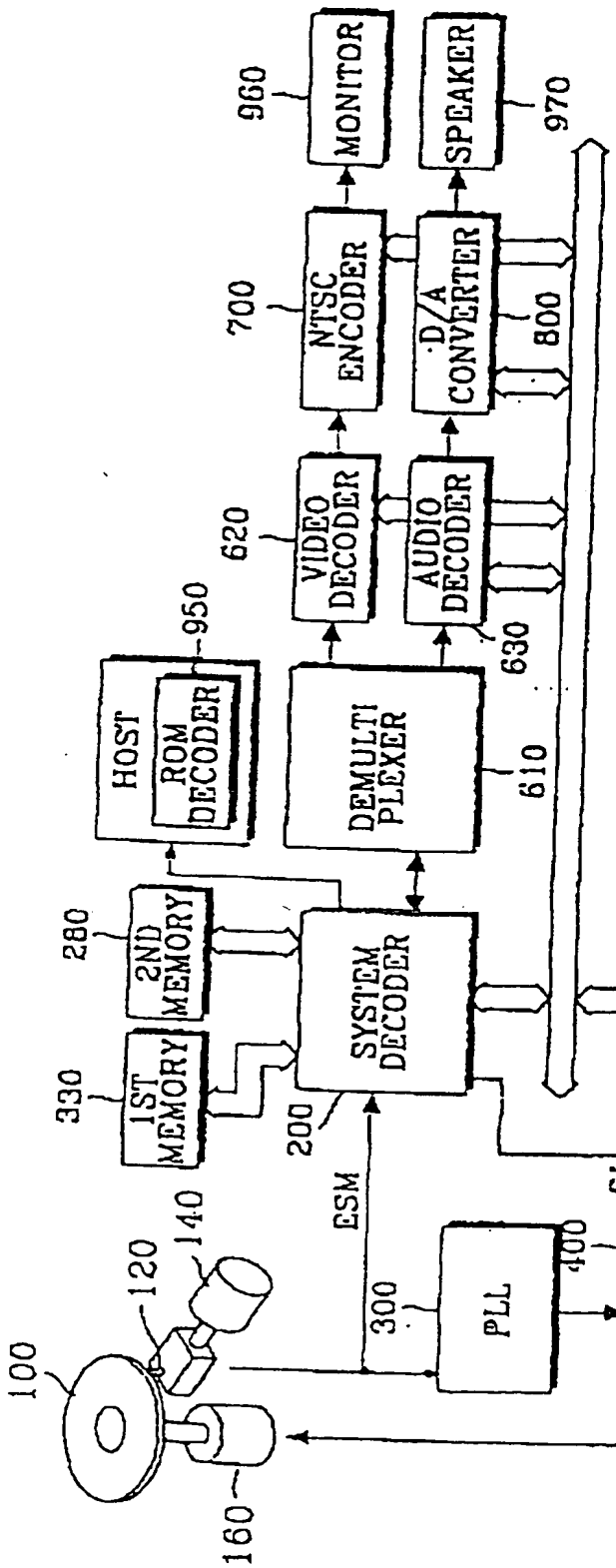


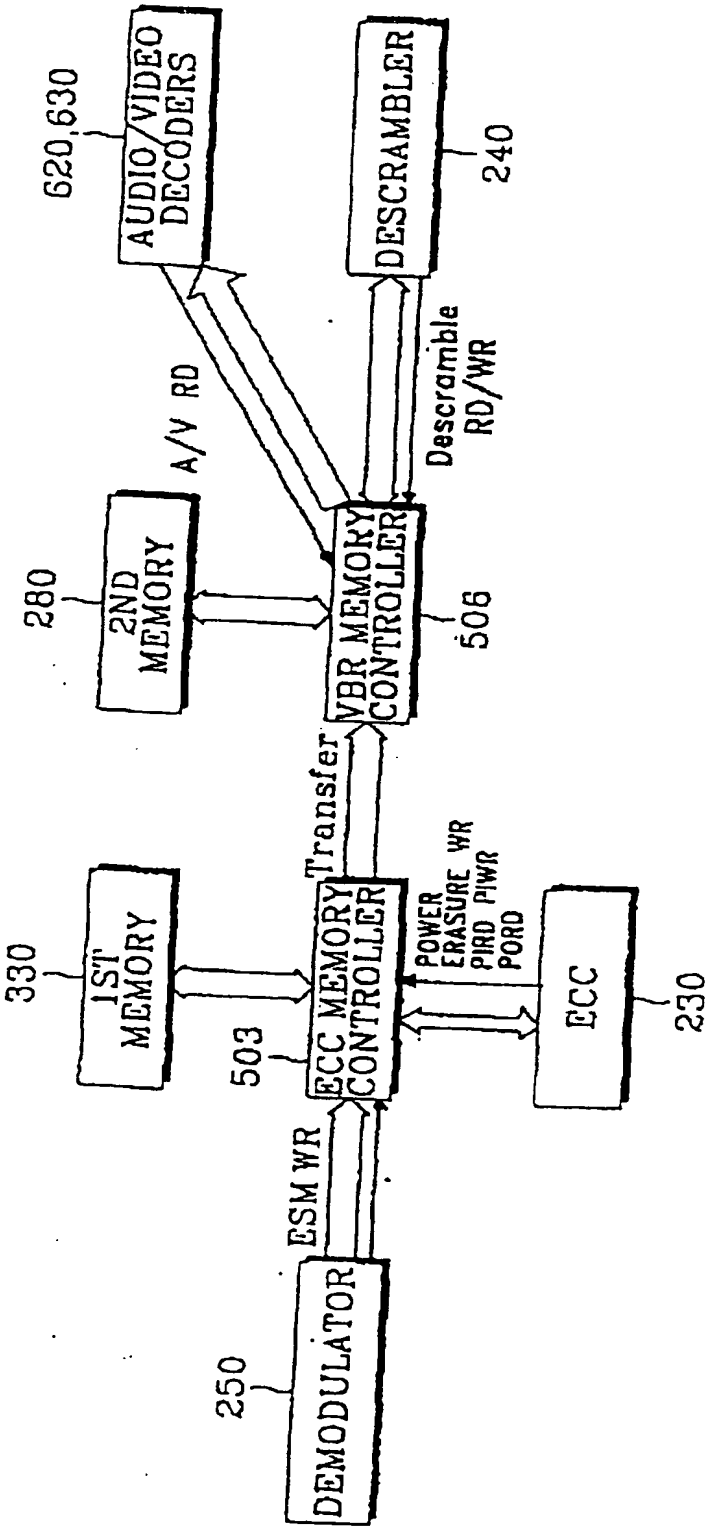
FIG. 4

GB 2 314 450 A



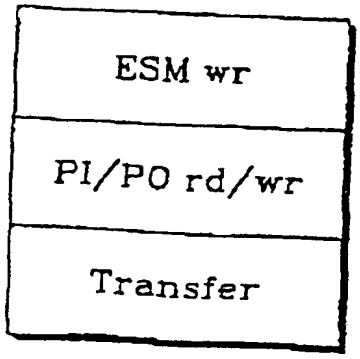
(PRIOR ART)

FIG. 1



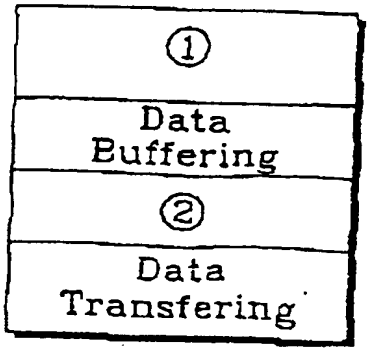
(PRIOR ART)

FIG. 2



(PRIOR ART)

FIG. 3A



(PRIOR ART)

FIG. 3B

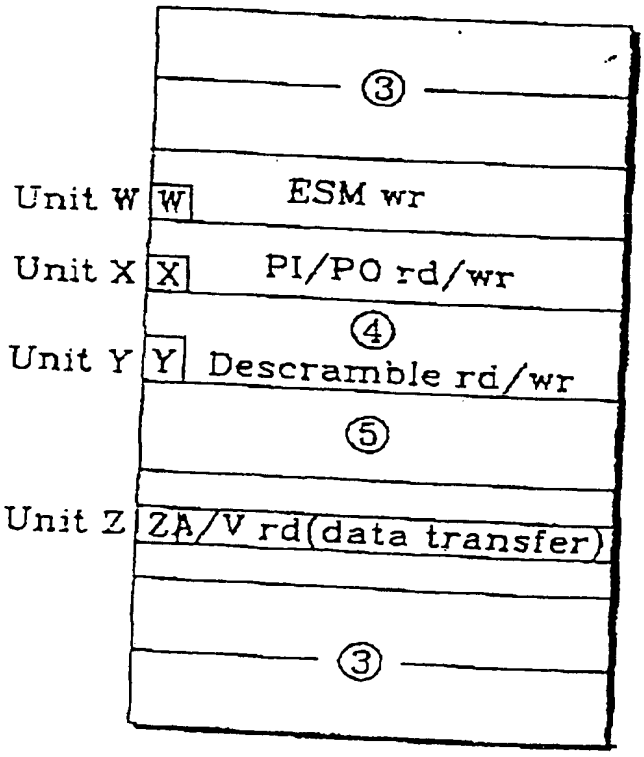


FIG. 6

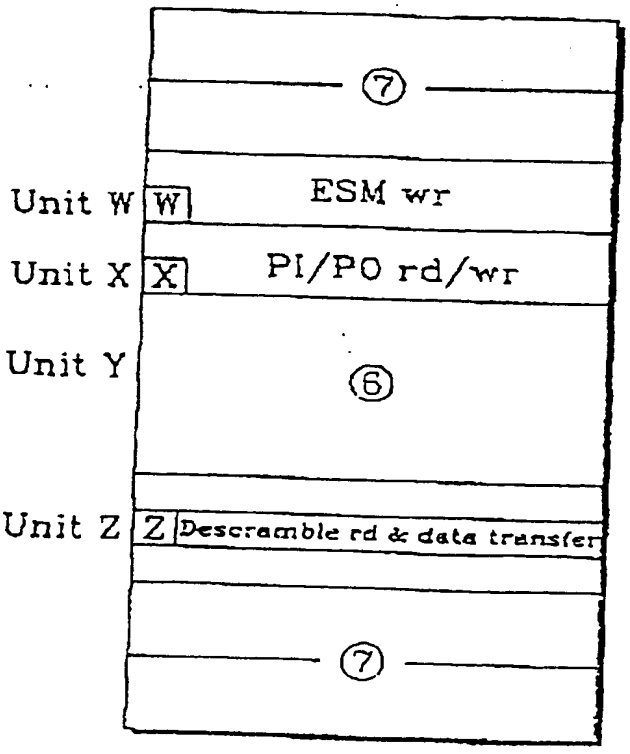


FIG. 8

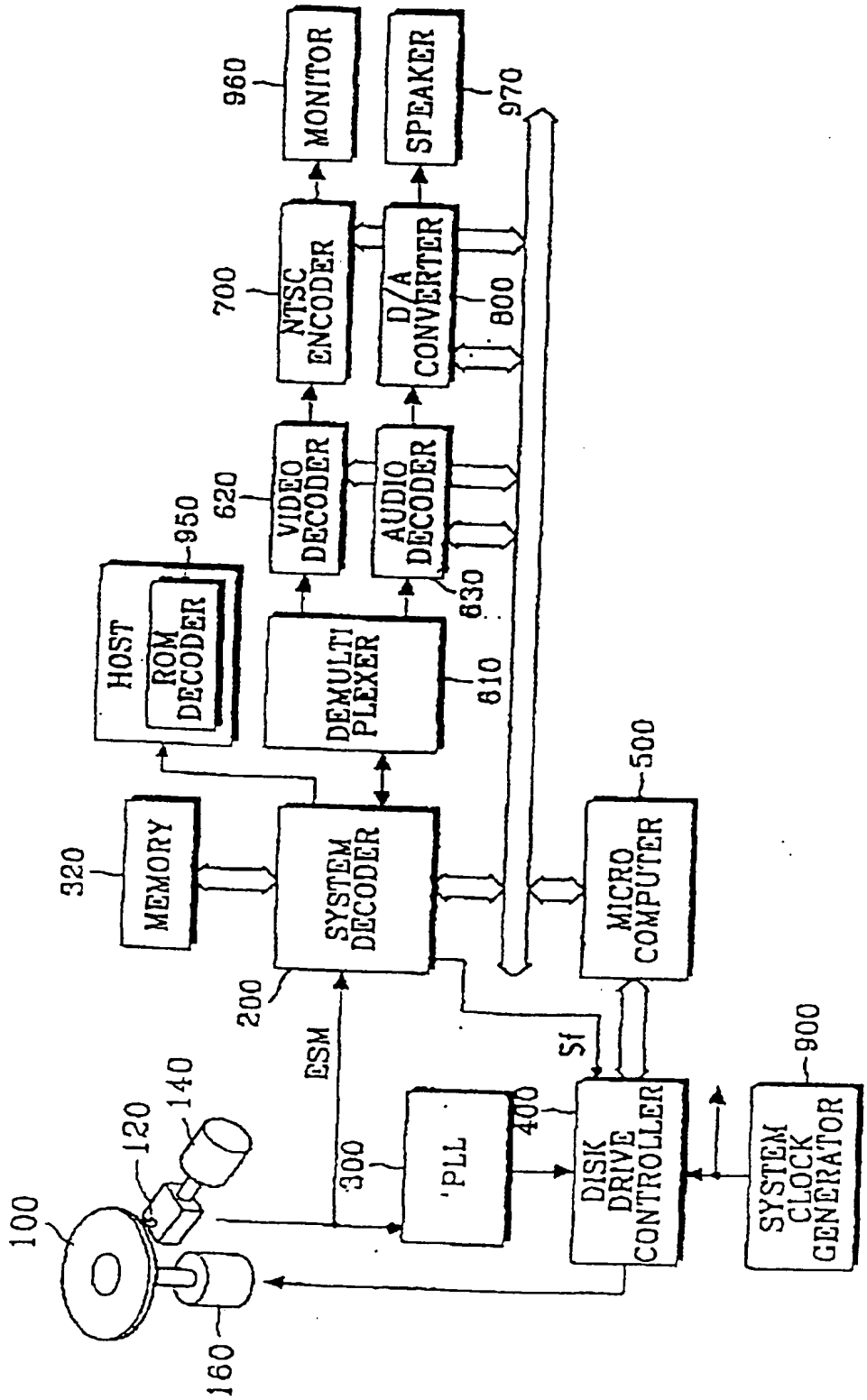

960
MONITOR
970
SPEAKER
700
NTSC ENCODER
D/A CONVERTER
800
620
VIDEO DECODER
AUDIO DECODER
630
950
HOST
ROM DECODER
DEMULTI PLEXER
810
320
MEMORY
SYSTEM DECODER
200
MICRO COMPUTER
500
ESM
SI
140
120
100
300
PLL
400
DISK DRIVE CONTROLLER
900
SYSTEM CLOCK GENERATOR
160

FIG. 4

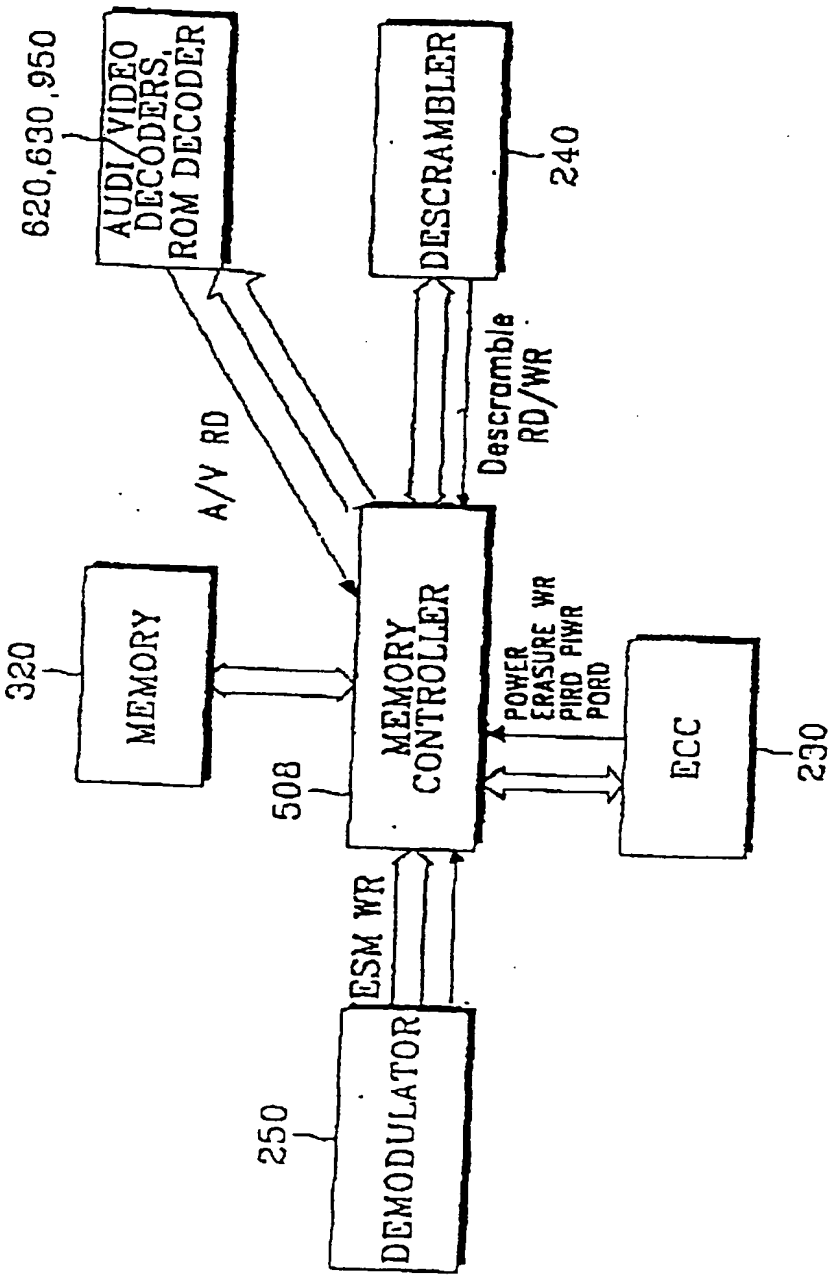

620,630,950
AUDI/VIDEO DECODERS, ROM DECODER
DESCRAMBLER
240
A/V RD
Descramble RD/WR
320
MEMORY
MEMORY CONTROLLER
508
POWER
ERASURE WR
PIRD PIWR
PORD
ECC
230
ESM WR
250
DEMODULATOR

FIG. 5

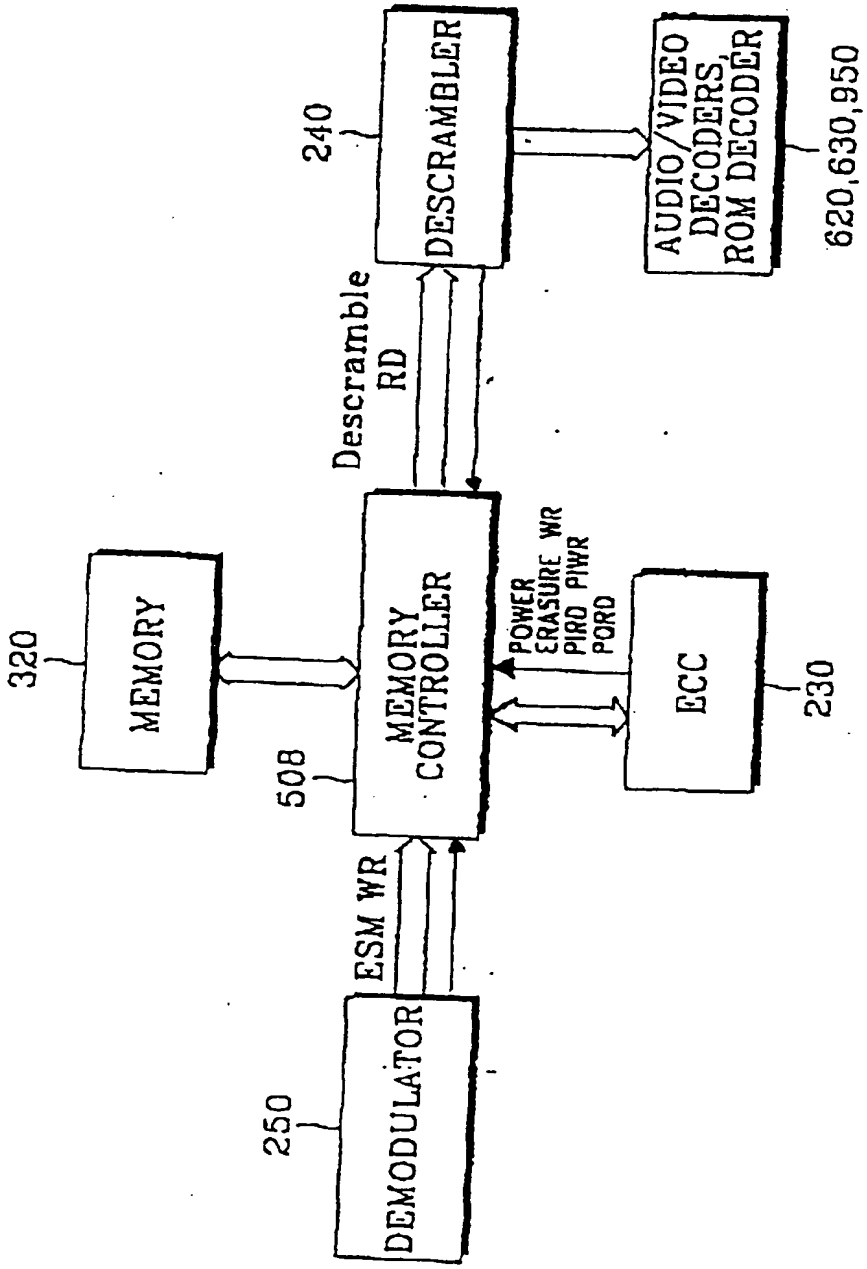

DEMODULATOR
250
ESM WR
MEMORY CONTROLLER
508
MEMORY
320
ECC
230
POWER
ERASURE WR
PIRD PIWR
PORD
Descramble RD
DESCRAMBLER
240
AUDIO/VIDEO DECODERS, ROM DECODER
620,630,950

FIG. 7

DEVICE FOR CONTROLLING MEMORY IN DIGITAL VIDEO DISK REPRODUCING DEVICE AND METHOD THEREFOR

The present invention relates to a device and method for controlling a memory, and more particularly to a device and method for controlling a memory in a digital video (or versatile) disk reproducing device.

A digital video disk, as a disk medium for a digital moving picture, is a cheap multimedia memory device capable of recording high quality video/audio data. Such digital video disks can store an MPEG2 (Moving Picture Experts Group 2) digital image of over 2 hour-quantity.

Referring to Figure 1, there is illustrated a general digital video disk reproducing device, in which a disk motor 160 rotates a disk 100 with a constant speed, and an optical pickup 140 with a head 120 reads a digital image on the disk 100 and converts the digital image into an analog high frequency (RF) signal. This signal is reshaped into a pulse, and a data stream ESM of the pulse is applied to a digital phase locked loop (hereinafter, referred to as "PLL") 300 and a system decoder 200. The digital PLL 300 includes a phase comparator, a voltage controlled oscillator and a frequency demultiplier, to generate a first clock synchronized with a signal reproduced from the disk 100. A disk drive controller 400 controls a constant linear velocity of the disk revolution and other disk operations according to a frame synchronous signal Sf supplied from a synchronization detector (not shown) of the system decoder 200, in the light of a frequency servo and a phase servo. First and second memories 330 and 280 are a 128Kb SRAM (Static Random Access Memory) and a 4Mb RAM, respectively. The former is used for an error correction, while the latter is used for

a VBR (Variable Bit Rate) buffer or a data buffer. The system decoder 200 demodulates the data read out from the disk 100 into the original state. The demodulated data is stored in the first memory 330 and read out by the block unit to correct errors at the system decoder 200. The error corrected data is stored again into the first memory 330. Further, the system decoder 200 descrambles the data read out from the first memory 330, to store the descrambled data into the second memory 280. The descrambled data is again read out from the second memory 280 and supplied to a demultiplexer 610. The demultiplexer 610, as a data parser, provides an AC3/MPEG audio decoder 630 with an audio signal and an MPEG2 video decoder 620 with a video signal, respectively. A microcomputer 500 controls an overall operation of the optical disk reproducing system, and generates a transfer control signal in response to a data transfer start signal from the audio decoder 630 or the video decoder 620. The audio and video data demodulated respectively at the audio decoder 630 and the video decoder 620 are provided to a speaker 970 and a monitor 960 through a digital-to-analog converter 800 and an NTSC (or PAL) encoder 700, respectively. A ROM (Read Only Memory) decoder 950 is commonly prepared in a host computer (e.g., a personal computer) and operates according to a control of the host computer. The ROM decoder 950 transfers data generated from the system decoder 200 to the host computer based on a predetermined interfacing method.

Referring to Figure 2, there is shown a detailed diagram of a section related to controlling the first and second memories 330 and 280. Referring to FIGs. 3A and 3B, there are shown detailed diagrams of the first and second memories 330 and 280, respectively.

The first memory 330, as an error correction buffer, includes three regions ESM_wr, PI/PO_rd/wr, and Transfer, as shown in Figure 3A. The region ESM_wr buffers 8-14 modulation data of the data stream ESM generated from the disk 100. The region PI/PO_rd/wr performs a PI/PO error correction with respect to an error correction block that has been buffered. The region Transfer is to transfer the error corrected data to the second memory 280. The second memory, as a VBR buffer, includes a region for buffering the error corrected data and another region for transferring data in accordance with a request from the audio and video decoders 620 and 630 or the ROM decoder 950, as shown in Figure 3B. Further, a reference numeral (1) represents an absolute value obtained by subtracting an address for buffering the error corrected data into the memory from an address for transferring data to the audio and video decoders 620 and 630 or the ROM decoder 950. A reference numeral (2) represents an absolute value obtained by subtracting an address for transferring data to the audio and video decoders 620 and 630 or the ROM decoder 950 from an address for buffering the error corrected data into the memory.

A demodulator 250 demodulates the input data stream ESM by the symbol unit of predetermined bit numbers. On the other words, the demodulator 250 applies the data stream ESM to a 32-bit shift register 211. Lower (or upper) 16 bits out of the 32-bit output from the 32-bit shift register 211 is transferred to a 16-8 demodulator 212. The 16-8 demodulator 212 converts the 16-bit data input into 8-bit data which constitutes the symbol. This operation should be performed, since the data has undergone the 8-16 modulation when being written on the disk 100.

An ECC (Error Correction Circuit) memory controller 503 controls an access to the first memory 330, in order to correct an error with respect to the demodulated data. An ECC 230 corrects an error in the row and column directions with respect to a predetermined error correction block including the data read from disks in a DVD (Digital Video Disk) system. It should be noted that in the application, the data are of (182, 172, 11) in row and (208, 192, 17) in column, respectively. Namely, lengths of the codeword are respectively 182 in row and 208 in column, lengths of main data excluding parity are respectively 172 in row and 192 in column, and intervals between the codewords are respectively 11 in row and 17 in column. In order to perform such error correction, the first memory 330 receives ID (Identification) data and main data generated from the demodulator 250 and stores those data by the block unit, so as to form the error correction block. The error correction block includes data for 16 sectors. Further, the first memory 330 also buffers the data while the error corrections are executed in the row and column directions, and stores the error corrected data.

A VBR memory controller 506 controls an access to the second memory 280 in order to VBR-buffer the error corrected data. Namely, the VBR memory controller 506 allows the second memory 280 to buffer the descrambled DVD data and transfer the buffered data to the audio and video decoders 620 and 630 according to the data transfer control signal generated from the microcomputer 500.

A descrambler 240 reads and descrambles the main data which has been scrambled prior to being written on the disk 100, to restore to the original data. The main data is 2Kbyte.

As can be appreciated from the above descriptions, the prior art DVD reproducing device includes the error correction memory and the VBR or data buffering memory separately. Accordingly, the memory controllers should be prepared separately, so that the structure may become complicated and the manufacturing cost may increase. As the result, it may be difficult to make the products compact.

It is therefore an aim of embodiments of the present invention to provide a compact digital video disk reproducing device including a single memory used both for an error correction and for a data buffering, and a method for controlling the same.

According to an aspect of the present invention, a method for controlling a memory in an optical disk reproducing device is provided, wherein the memory is accessed to read or write data while performing a modulation, an error correction, a deinterleaving, a descrambling and transferring the data to audio/video decoders or a ROM decoder with respect to the data read from an optical disk, the method including the steps of: designating a unit number to each sector of the memory; determining first, second and third regions, the first region corresponding to an absolute value of a unit number obtained by subtracting a unit number Y of a sector where a data read/write operation is completed during the descrambling from a unit number X of a start sector in an error correction block where the error correction is completed, the second region corresponding to an absolute value of a unit number obtained by subtracting a unit number Z of a sector where the data is completely transferred to the audio/video decoders or the ROM decoder from the unit number Y, the third region corresponding to

an absolute value of a unit number obtained by subtracting the unit number Z from a unit number W of a sector where a writing operation of demodulated data is completed; and controlling a W-pointer and a Z-pointer not to overfull a Z-pointer and a Y-pointer respectively, and controlling an X-pointer and the Y-pointer not to pass ahead the W-pointer and the X-pointer respectively.

According to another aspect of the present invention, there is provided a method for controlling a memory in an optical disk reproducing device, wherein the memory is accessed to read or write data while performing a modulation, an error correction, a deinterleaving, a descrambling and transferring the data to audio/video decoders or a ROM decoder with respect to the data read from an optical disk, includes the steps of: designating a unit number to each sector of the memory; determining first and second regions, the first region corresponding to an absolute value of a unit number obtained by subtracting a unit number Z of a sector where the descrambling and the data transferring to the audio/video decoders or the ROM decoder are completed from a unit number X of a start sector in an error correction block where the error correction is completed, the second region corresponding to an absolute value of a unit number obtained by subtracting the unit number Z from a unit number W of a sector where demodulated data is completely written into a buffer; and controlling a W-pointer and a Z-pointer not to overfull a Z-pointer and a Y-pointer respectively, and controlling an X-pointer not to pass ahead the W-pointer.

For a better understanding of the invention, and to show how embodiments of the same may be carried into

effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 is a schematic block diagram of a digital video disk reproducing device according to the prior art;

Figure 2 is a detailed diagram of a section related to controlling memories shown in Figure 1;

FIGs. 3A and 3B are diagrams showing first and second memories shown in Figure 1, respectively;

Figure 4 is a schematic block diagram of a digital video disk reproducing device according to an embodiment of the present invention;

Figure 5 is a detailed diagram of a section related to controlling a memory shown in Figure 4 according to a first embodiment of the present invention;

Figure 6 is a diagram for explaining how a memory buffer is managed while a memory controller shown in Figure 5 processes various request signals;

Figure 7 is a detailed diagram of a section related to controlling a memory shown in Figure 4 according to a second embodiment of the present invention; and
Figure 8 is a diagram for explaining how a memory buffer is managed while a memory controller shown in Figure 7 processes various request signals.

A preferred embodiment of the present invention will be described in detail hereinbelow with reference to the attached drawings, in which like reference numerals represent like elements. Further, it should be clearly

understood by those skilled in the art that many specifics such as the detailed circuit elements are shown only by way of example to bring a better understanding of the present invention and the present invention may be embodied without those specifics. Moreover, it should be noted that detailed descriptions on the related prior art may be intentionally omitted if it is believed to be unnecessary in describing the concepts of the present invention.

Referring to Figure 4, there is illustrated a digital video disk reproducing device according to an embodiment of the present invention. It is shown in the drawing that the digital video disk reproducing device includes a single memory 320 and other structures are the same as those of the prior art device shown in Figure 1. Namely, the memory 320 performs the error correction as well as the VBR or data buffering.

Referring to Figure 5, there is shown a detailed diagram of a section related to controlling the memory 320 shown in Figure 4 according to a first embodiment of the present invention. The memory 320 is used both for the error correction and for the VBR or data buffering. A demodulator 250 demodulates the input data stream ESM by the symbol unit of predetermined bit numbers. On the other words, the demodulator 250 applies the data stream ESM to a 32-bit shift register 211. Lower (or upper) 16 bits out of the 32-bit data output from the 32-bit shift register 211 is transferred to a 16-8 demodulator 212. The 16-8 demodulator 212 converts the 16-bit data input into 8-bit data which constitutes the symbol. This operation should be performed, since the data has undergone the 8-16 modulation when being written on the disk 100.

An ECC 230 corrects an error in row and column directions with respect to a predetermined error correction block including the data read from disks in the DVD (Digital Video Disk) system. It should be noted that in the application, the data are (182, 172, 11) in row and (208, 192, 17) in column, respectively. Namely, lengths of the codeword are respectively 182 in row and 208 in column, lengths of main data excluding parity are respectively 172 in row and 192 in column, and intervals between the codewords are respectively 11 in row and 17 in column. In order to perform such error correction, the memory 320 receives ID data and main data generated from the demodulator 250 and stores those data by the block unit, so as to form the error correction block. The error correction block includes data for 16 sectors. Further, the memory 320 also buffers the data while the error corrections are executed in the row and column directions, and stores the error corrected data.

A descrambler 240 reads and descrambles the main data which has been scrambled prior to being written on the disk, to restore to the original data. The main data is 2Kbyte.

A memory controller 508 controls an access to the memory 320, in order to correct an error with respect to the demodulated data. Furthermore, the memory controller 508 controls an access to the memory 320, so as to descramble the error corrected data. Namely, the memory controller 508 reads data to be descrambled from the memory 320 and/or allows the memory 320 to buffer the descrambled data and transfer the buffered data to the audio and video decoders 620 and 630 or the ROM decoder 950 according to the data transfer control signal generated from the microcomputer 500. The audio and video

decoders 620 and 630 or the ROM decoder 950 generate a transfer request signal A/V_RD, so as to cause the microcomputer 500 to generate the transfer control signal to the memory controller 508.

Referring to Figure 6, there is shown a diagram for explaining how a memory buffer is managed while the memory controller 508 shown in Figure 5 processes various request signals. In the drawing, a letter "W" represents a unit number (i.e. memory area) of a sector where the 8-16 demodulated data has been stored into the buffer; a letter "X" a unit number of a sector where the error correction has been completed; a letter "Y" a unit number of a sector where the descrambling has been completed; a letter "Z" a unit number of a sector where the data is completely transferred to the audio and video decoders 620 and 630 or the ROM decoder 950.

Meanwhile, a reference numeral (4) represents a region corresponding to an absolute value of the unit number obtained by subtracting the unit number "Y" of the sector where the descrambler 240 has completed the data read/write operation, from the unit number "X" of a start sector of an error corrected block where the error correction has been completed. A reference numeral (5) represents a region corresponding to an absolute value of the unit number obtained by subtracting the unit number "Z" of the sector where the data has been completely transferred to the audio and video decoders 620 and 630 or the ROM decoder 950, from the unit number "Y" of the sector where the descrambler 240 has completed the data read/write operation. Further, a reference numeral (3) represents a region corresponding to an absolute value of the unit number obtained by subtracting the unit number "Z" of the sector where the data has been completely

transferred to the audio and video decoders 620 and 630 or the ROM decoder 950, from the unit number "W" of the sector where the demodulated data has been completely stored into the buffer.

Here, the buffer is managed such that a W-pointer should not overfull a Z-pointer (memory overfull state), [in this respect the term to "overfull" a pointer would mean overwriting data, such as ESM data, by the Z pointer passing ahead of the W pointer, before data has been able to be output to audio/video decoders] and the Z-pointer should not overfull a Y-pointer (memory empty state). In order to secure such buffer management, the system decoder 200 notifies buffer states, such as a memory overfull state and a memory underfull state, to the microcomputer 500. Further, the system decoder 200 automatically controls the X-pointer and the Y-pointer not to pass ahead the W-pointer and the X-pointer, respectively. Here, a standard unit of the unit numbers is assumed to be 2Kbyte which is a standard unit for the memory management.

Referring to Figure 7, there is shown a detailed diagram of a section related to controlling the memory 320 shown in Figure 4 according to a second embodiment of the present invention. When compared with the first embodiment shown in Figure 5, the second embodiment is different only in that the descrambler 240 and the audio/video decoders 620 and 630 or the ROM decoder 950 do not generate the request signals described hereinbelow to the memory controller 508.

As illustrated in Figure 7, the audio/video decoders 620 and 630 or the ROM decoder 950 receive the descrambled data directly from the descrambler 240. Thus, it is not necessary that the audio/video decoders 620 and 630 or the

ROM decoder 950 generate the transfer request signal A/V_RD to the memory controller 508. Accordingly, the descrambler 240 does not need to generate the write request signal (Descramble_WR) to the memory controller 508.

Referring to Figure 8, there is shown a diagram for explaining how a memory buffer is managed while the memory controller 508 shown in Figure 7 processes various request signals. In the drawing, a reference numeral (6) represents a region corresponding to an absolute value of a unit number obtained by subtracting the unit number "Z" of the sector where the descrambling and the data transferring are completed, from the unit number "X" of a start sector in an error correction block where the error correction is completed. A reference numeral (7) represents a region corresponding to an absolute value of a unit number obtained by subtracting the unit number "Z" of the sector where the descrambling and the data transferring are completed, from the unit number "W" of the sector where the demodulated data is completely written into the buffer.

Here, the buffer is managed such that the W-pointer should not overfull the Z-pointer (memory overfull state) and the Z-pointer should not overfull the Y-pointer (memory empty state). In order to secure such buffer management, the system decoder 200 notifies buffer states, such as a memory overfull state and a memory underfull state, to the microcomputer 500. Further, the system decoder 200 automatically controls the X-pointer not to pass ahead the W-pointer.

As described above, the digital video disk reproducing device according to embodiments of the present

invention includes a single memory used both for the error correction and for the data buffering, so that the manufacturing cost may be reduced and the circuit structure may be simplified.

Although various preferred embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the art will still fall within the scope of the present invention as defined in the appended claims.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS

1. A method for controlling a memory in an optical disk reproducing device, wherein the memory is accessed to read or write data while performing a modulation, an error correction, a deinterleaving, a descrambling and transferring the data to audio/video decoders or a ROM decoder with respect to the data read from an optical disk, comprising the steps of:

designating a unit number to each sector of the memory;

determining first, second and third regions, said first region corresponding to an absolute value of a unit number obtained by subtracting a unit number Y of a sector where a data read/write operation is completed during the descrambling from a unit number X of a start sector in an error correction block where the error correction is completed, said second region corresponding to an absolute value of a unit number obtained by subtracting a unit number Z of a sector where the data is completely transferred to the audio/video decoders or the ROM decoder from said unit number Y, said third region corresponding to an absolute value of a unit number obtained by subtracting said unit number Z from a unit number W of a sector where a writing operation of demodulated data is completed; and

controlling a W-pointer and a Z-pointer not to overfull a Z-pointer and a Y-pointer respectively, and controlling an X-pointer and the Y-pointer not to pass ahead the W-pointer and the X-pointer respectively.

2. A method for controlling a memory in an optical disk reproducing device, wherein the memory is accessed to read or write data while performing a modulation, an error correction, a deinterleaving, a descrambling and transferring the data to audio/video decoders or a ROM decoder with respect to the data read from an optical disk, comprising the steps of:

designating a unit number to each sector of the memory;

determining first and second regions, said first region corresponding to an absolute value of a unit number obtained by subtracting a unit number Z of a sector where the descrambling and the data transferring to the audio/video decoders or the ROM decoder are completed from a unit number X of a start sector in an error correction block where the error correction is completed, said second region corresponding to an absolute value of a unit number obtained by subtracting said unit number Z from a unit number W of a sector where demodulated data is completely written into a buffer; and

controlling a W-pointer and a Z-pointer not to overfull a Z-pointer and a Y-pointer respectively, and controlling an X-pointer not to pass ahead the W-pointer.

3. A method substantially as herein described with reference to Figures 4 to 6.

4. A method substantially as herein described with reference to Figures 4, 7 and 8.

The Patent Office

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Application No: GB 9712908.4
Claims searched: 1 and 2

Examiner: Peter Easterfield
Date of search: 20 August 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): G5R (RGC, RHX)

Int Cl (Ed.6): G11B 20/10

Other: Online: WPI, JAPIO, CLAIMS

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
	None	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.